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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,656	01/23/2004	Chien-Ping Huang	60702 (71987)	9385

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,656	HUANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 15 -20 is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3 – 5, 8, and 10 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang et al. (US 6,590,269 B1) in view of Huang (6,635,209 B2).

3. Regarding Claim 1, Chuang et al. disclose a semiconductor package with a photosensitive chip, comprising:

a substrate having a core (30) (Figure 4) with a plurality of conductive traces (Col. 2, lines 59 – 61) having a terminal (Figure 4, on surface 38 connected to wire 43),

at least one photosensitive chip (34) mounted on the substrate and electrically connected to the exposed terminals of the conductive traces (Figure 4, on surface 38 connected to wire 43),

an encapsulation dam (frame layer) (32) formed on the peripheral portion of the core (30) and surrounding the chip (34), wherein the dam comprises a support portion (near 46) having a height greater than a thickness of the chip (34), and

a lid (36) attached to the support portion of the dam (32) for sealing the dam such that the chip (34) is received in a space defined by the substrate, the dam, and the lid.

Chuang et al. do not disclose the presence of a solder mask layer covering the conductive traces and allowing a portion to be exposed as terminals and formed with an opening to expose a peripheral portion on the surface of the core (substrate). In like manner, Chuang et al. do not disclose the presence of a shoulder portion of an encapsulation (dam) structure wherein the shoulder is adjacent and flush with the solder mask layer.

Huang discloses the presence of a solder mask layer (122) (Figure 5A) that covers the conductive traces (130), allowing the terminals to be exposed outside the solder mask layer and a peripheral portion on the surface of the core (substrate) to be exposed (peripheral left and right regions). Further, Huang discloses the presence of an encapsulation "shoulder" (122a) (Figure 5B) adjacent and flush with the solder mask layer (122). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the solder mask layer and the encapsulation "shoulder" of Huang in Chuang et al. to provide protection to adjacent parts of the chip and a sealant at the edge zones.

4. Regarding Claims 3 and 4, Chuang et al. do not disclose the the presence of a shoulder portion of the dam with a width in the range, 0.1 to 1.0 mm. Huang discloses that the width of the shoulder region (122a) is in the range, 0.4 to 1.2 mm (Col. 5, lines 17 – 23), which is consistent with the values recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Huang with Chuang et al. to provide an edge structure providing sealing.

5. Regarding Claim 5, Chuang et al. disclose that each of the terminals (Figure 4, at surface 38, left and right) serves as a bond finger where a bonding wire (43) is bonded to electrically con-

nect the chip to the substrate.

6. Regarding Claim 8, Chuang et al. disclose a fabrication method of a semiconductor package with a photosensitive chip, comprising the steps of:

preparing a substrate having a core (30) (Figure 4) with a plurality of conductive traces (Col. 2, lines 59 – 61) having a terminal (Figure 4, on surface 38 connected to wire 43),

forming an encapsulation dam (frame layer) (32) formed on the peripheral portion of the core (30) and surrounding the chip (34), wherein the dam comprises a support portion (near 46) having a height greater than a thickness of the chip (34), and

mounting at least one photosensitive chip (34) mounted on the substrate and electrically connected to the exposed terminals of the conductive traces (Figure 4, on surface 38 connected to wire 43),

attaching a lid (36) attached to the support portion of the dam (32) for sealing the dam such that the chip (34) is received in a space defined by the substrate, the dam, and the lid.

Chuang et al. do not disclose applying a solder mask layer covering the conductive traces and allowing a portion to be exposed as terminals and formed with an opening to expose a peripheral portion on the surface of the core (substrate). In like manner, Chuang et al. do not disclose forming a shoulder portion of an encapsulation (dam) structure wherein the shoulder is adjacent and flush with the solder mask layer.

Huang discloses applying a solder mask layer (122) (Figure 5A) that covers the conductive traces (130), allowing the terminals to be exposed outside the solder mask layer and a

peripheral portion on the surface of the core (substrate) to be exposed (peripheral left and right regions). Further, Huang discloses the formation of an encapsulation "shoulder" (122a) (Figure 5B) adjacent and flush with the solder mask layer (122). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures for forming a solder mask layer and the encapsulation "shoulder" of Huang in Chuang et al. to provide protection to adjacent parts of the chip and a sealant at the edge zones.

7. Regarding Claims 10 and 11, Chuang et al. do not disclose a fabrication method wherein the shoulder portion of the dam has a width in the range of 0.1 to 1.0 mm. Huang discloses that the width of the shoulder region (122a) is in the range, 0.4 to 1.2 mm (Col. 5, lines 17 – 23), which is consistent with the values recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Huang with Chuang et al. to provide an edge structure providing sealing.

8. Regarding Claim 12, Chuang et al. disclose a fabrication method wherein each of the terminals (Figure 4, at surface 38,left and right) serves as a bond finger where a bonding wire (43) is bonded to electrically connect the chip to the substrate.

9. Claims 2, 6, 7, 9, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang et al. in view of Huang, as applied to Claims 1, 3 - 5, 8, and 10 - 12, and further in view of Nakazawa et al. (US 6,448,665 B1).

10. Regarding Claim 2, Chuang et al. do not disclose a semiconductor package comprising a plurality of solder balls implanted on a side of the substrate opposite to the side mounted with the chip. Nakazawa et al. disclose a semiconductor package, wherein the solder balls (18) (Figure 3) are located on the opposite side of the substrate from the chip mounting side. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Nakazawa et al. with Chuang et al. to obtain a means of providing signal transfer between external contacts and the chip.

11. Regarding Claims 6 and 7, Chuang et al. do not disclose a semiconductor package wherein the core (substrate) is made of an epoxy resin and the dam (mold layer) is made of an epoxy based polymer resin. Nakazawa et al. disclose thaty the core is made of epoxy resin and the dam is made of an epoxy based polymer resin (Col. 9, lines 49 - 54). It w3ould have been obvious to one of ordinary skill in the art at the time of the invention to combine Nakazawa et al. with Chuang et al. to opbtain durable materials for the semiconductor package.

12. Regarding Claim 9, Chuang et al. do not disclose a fabrication method of a semiconductor package wherein a plurality of solder balls are implanted on the opposite side of the substrate from the chip mounting side. Nakazawa et al. disclose a fabrication method, wherein the solder balls (18) (Figure 3 are located on the opposite side of the substrate from the chip mounting side.

13. Regarding Claims 13 and 14, Chuang et al. do not disclose a fabrication method, wherein the core (substrate) is made of an epoxy resin and the dam (mold layer) is made of an epoxy based polymer resin. Nakazawa et al. disclose thaty the core is made of epoxy resin and the dam is made of an epoxy based polymer resin (Col. 9, lines 49 - 54). It w3ould have been obvious to one of ordinary skill in the art at the time of the invention to combine Nakazawa et al. with Chuang et al. to obtain durable materials for the semiconductor package.

Allowable Subject Matter

14. Claims 15 - 20 are allowed. The prior art of record do not reasonably teach or suggest, either singularly or in combination, the limitation in Claim 15 of "*forming an encapsulation body comprising a plurality of interconnected encapsulation dams each on the peripheral portion of the corresponding substrate, wherein each of the encapsulation dams comprises a shoulder portion adjacent to and flush with the solder mask layer, and a protruded support portion surrounding the shoulder portion and forming a space encompassed by the dam, the adjacent dams having the support portions thereof interconnected.*"

Conclusions

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee,** whose telephone number is **(571) 272.1658.** The Examiner can normally be reached on Monday through Friday from 8:30 AM to 5 PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor,

Eddie Lee, can be reached on **(571) 272-1732.** The fax number for the organization where this application is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
November 8, 2004